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DESIGN OF SPACE AND EVIATION APPLICATIONS USING RHBD AND 12T SRAM MEMORY

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Abstract: In this study, we examine the various fault-tolerance strategies used in SRAM cell architectures. Different circuit-level strategies have been used due to the fact that SRAM cells are vulnerable to radiation-induced single-event upsets. One alternative to the standard SRAM cell circuits is to include extra transistors to provide redundant storage nodes. Different design techniques are analyzed and evaluated in relation to the strengths and weaknesses of SRAM cells in terms of different performance parameters like as speed, area, power, stability, fault tolerance, etc. The panel agrees that in the future, it will be crucial to create an SRAM cell design that reduces the tension between read/write speed and SEU tolerance.

Keywords: static random-access memory; protection from radiation; single-event upset

1. Introduction

large improvements in current drivability and a large decrease in parasitic capacitances of transistors have occurred as technology has scaled down. As a result, digital circuits become faster, use less energy, and take up less space. However, it is much simpler to alter the voltage of circuit nodes in digital circuits due to the much lower quantity of charge encoding a logic value. That is, the signals in digital circuits are very vulnerable to environmental disturbances. Radiation may cause energetic ionized particles in the environment, and these particles can have enough charge to overwrite memory in a digital device. As a consequence, the circuit functioning is more likely to encounter a logical fault.

The static random-access memory (SRAM) cell, a hardware component that stores data as logical values, is particularly susceptible to this kind of error in digital circuits. Data recorded in a standard 6 T SRAM cell is readily inverted by a radiation-induced charge particle due to the cell's simple cross-coupled inverter architecture. Methods of improving fault tolerance may be implemented at the device, layout, circuit, or system levels of design. Among these methods, modifying the SRAM cell's structure on the circuit level to make its storage nodes less susceptible to external charge shocks while maintaining the cell's original stored voltage is the most promising.

There are a plethora of radiation-resistant SRAM architectures under development. It is common practice to use more transistors in a more intricate fashion than is required by 6 T SRAM in order to make the SRAM cell resilient to the radiation-induced charge noise. There will be costs in terms of space, energy consumption, speed, and reliability of operation. It's helpful to compare different SRAM cell designs to see how they function in different situations.

This paper's remaining sections are structured as follows. Radiation-induced noise causes errors in the circuit components, which are discussed in Section 2, along with some possible solutions to this problem. In Section 3, we cover the different architectures of SRAM cells in depth. Section 4 compares and discusses the SRAM cell designs provided in Section 3.

2. Background

2.1. Soft Error and Single Event Transient (SET)

Permanent physical faults in the hardware may arise due to mistakes in the manufacturing process or circuit design error, causing a malfunction or error in the functioning of the electronic device. This is what technicians term a "hard error" in a digital gadget. It has been found that data bits are spontaneously or dynamically altered to wrong values, due to numerous noise sources impacting the electronic device after production, even in hardware free from this hard mistake. When contrasted with the hard mistake, this kind of blunder is called a "soft error" since it cannot be reproduced, does no damage, and has no long-term effects. Intermittent faults and transient faults are two forms of soft errors [1]. Faults in the intermittency of a structure occur at sporadic intervals and often in the same places. Power supply noise, temperature fluctuations, component aging, and signal coupling of parasitic capacitances are all contributors to intermittent defects. Due to improvements in both design and production methods, intermittent faults are now less of a problem in cutting-edge technology. Transient errors, however, are far more random, unexpected, and inevitable, and are often induced by cosmic rays and alpha particles. Accidental atmospheric impact by alpha particles or high-energy neutrons may cause charges to be generated in the transistors of an electrical device. The nodes' voltages may then be flipped to the wrong state, leading to a logical mistake.

The diffusion nodes (drain or source) of "off" transistors in integrated circuits are particularly vulnerable to the voltage shift caused by particle impact. The following steps depict the process by which the voltage shifts. Electron-hole pairs are created close to the p-n junction of the source or drain diffusion if an energetic particle contacts a source or drain node and then travels through the transistor. When a particle is injected into a material, the depletion zone of the p-n junction expands along its route, creating a strong electric field. As a result, a temporal junction current is produced when the electric field collects the created carriers (electrons and holes). This current causes an instantaneous drop or rise in voltage at the node acting as either source or drain. For instance, the node voltage is drastically reduced in an off nMOSFET because the source or drain is n+-doped, causing electrons to be drawn to the

n+ side. One term for this occurrence is "single event transient" (SET). SET may cause the node voltage of a pMOSFET with a p+-doped drain or source to rise accidentally.

2.2. Radiation-Hardening Strategies and Single-Event-Upset (SEU) Design

By altering the digital value at the storage nodes, SET may cause a data flip (from 0 to 1 or vice versa) in a digital circuit's memory. The process through which SET modifies a logical value is called a single-event upset (SEU). Figure 1 depicts a typical 6 T SRAM cell, in which the storage nodes Q and QB serve as drains for not only the nMOSFET access transistors (MX1,2) and pull-down transistors (MD1,2), but also the pMOSFET pull-up transistors (MU1,2). Therefore, both 0 1 and 1 0 SET polarities are available at the Q and QB nodes. By collecting charge in such a way that it results in 1 0 SET at the Q node, for instance, the value "1" may be stored when Q = VDD and QB = 0 V. This results in the QB node going from 0 V to VDD, which flips the data in the memory cell from "0" to "1." There have been a number of radiation-hardening design strategies developed to increase the resilience to SEU.

To begin, layout-level approaches such as shallow trench iso- lation, H-gate, and enclosed annular gate may be used, as shown in [2-4]. SEU may be mitigated by physically separating the charge injection node from the charge collecting node using a shallow trench isolation technique. H-gate and annular-gate based layouts are effective in reducing leakage current because of the gates' distinctive shapes. However, in today's age of sub-nanotechnology, these methods are not likely to be useful because of the stringent design requirements.

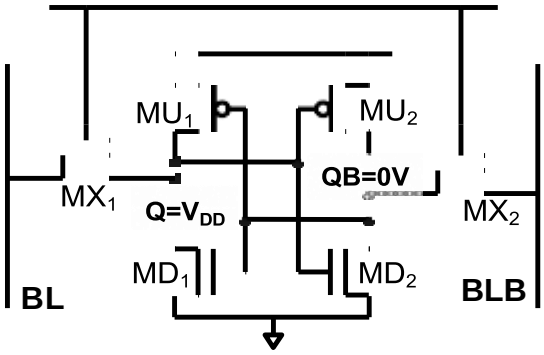

Figure 1. Schematic of the conventional 6 T SRAM cell.

One of the most popular traditional circuit-level radiation-hardened design strategies [5] is the triple modular redundancy (TMR). By using three identical memory cells, TMR ensures that all of the operation's data is safely stored. In a majority voting circuit, the data that is most often read out takes precedence. In this way, if a single cell experiences data corruption due to SEU, the other two copies will still have the right information, unaltered from their original states. The accuracy of the final results is ensured by a voting procedure. However, there is a large space and power cost because of the need to implement and run three copies of hardware.

The error correcting code (ECC) is the most well-known method of radiation-hardening design at the system level [6-11]. One or more bits of error may be identified and fixed by decoding the data during the read-accessing phase, after the multi-bit word data has been written after being encoded according to a specified pre-determined strategy. When SEU flips certain bits of a word, the bit sequencing of the word no longer conforms to the established pattern. Examining the specific way in which the word deviates from the norm enables one to zero down on the offending byte. There is a substantial delay and power penalty associated with using ECC because of the complexity of the encoding and decoding circuitry required.

Instead of using the standard 6 T SRAM cell, designing a new hardened SRAM cell has become one of the most popular ways to increase SEU's resilience. The new radiation-hardened SRAM cell design is implemented without changing the rest of the architecture or the peripheral circuits and systems. Using the new memory cell architecture is effective in terms of efficiency and performance compared to the alternatives. The next part will detail the construction, operation, and critical performance aspects of many different SRAM cell designs for radiation hardening.

3. Radiation-Hardened SRAM Cell Design

3.1. Dual Interlocked Storage Cell (DICE)

One of the most common radiation-resistant SRAM cells, 12 T DICE [12], is shown in schematic form in Figure 2. There are four nodes (A, B, C, and D) to store the information, as opposed to only two in a standard 6 T SRAM cell. Nodes A and C must share the same logic level, whereas nodes B and D must share the same level. A = C = VDD and B = D = 0 V when the cell stores a "1" at VDD, for instance. With WL = VDD, the storage nodes are connected to the bit-line pairs BL and BLB for the read/write operation, and WL is held at 0 for the hold operation. The read and write operations are carried out in the same way as in a regular 6 T SRAM cell. The information in storage is sent to BL and BLB to be read. The external write driver first turns on BL and BLB, and then the data are sent to the storage node through the access transistors.

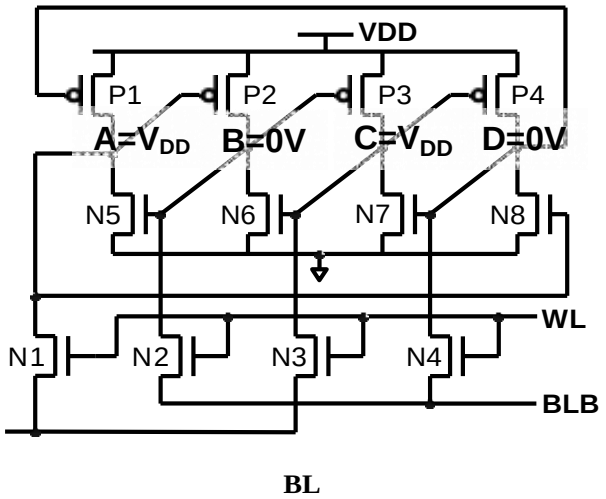

Figure 2. Schematic of 12 T DIEC SRAM cell.

Each storage node in DICE is powered by two nearby storage nodes, one of which controls the pFET and the other the nFET. For instance, pFET P1 and nFET N5, whose gates are linked to D and B, are responsible for driving A. Due to its one-of-a-kind setup, the cell can't make mistakes even if one of its nodes goes down.

DICE has the following SEU recovery behavior. The values A = C = VDD and B = D = 0 V are used to store the digit "1" in memory. When this happens, the voltage on A might drop from VDD to 0. This activates P2, which begins to increase B. Since C is still VDD, N6 remains on, preventing B from being pulled up to its full potential. And because D has not changed from 0 V, P1 stays on. So, P2 releases its grip on B and A is returned to VDD. Even if an unexpected incident brings down node A, the data will stay as "1" in storage because of this.

Overhead in terms of space and energy requirements will inevitably increase by a factor of around 2-2.5. DICE also fails to avoid data reversal when numerous nodes are concurrently perturbed.

We also have the Write-Enhanced Quatro-12 T Cell (WE-Quatro-12 T) and the Qud-Node 10 T (also known as the Quatro-10 T)

The Quatro-10 T cell, as described in [13], is shown in Figure 3a. A, B, C, and D nodes inside the cell serve as storage locations, much as DICE. A = D = 0 V and B = C = VDD are the values saved for the digit "1" in this case. In contrast to DICE, only two nodes (A and B) have access transistors (N5 and N6) that link them to differential bit-lines. Nodes (C and D) do not. Turned-on access transistors at WL = VDD execute the read operation by creating differential bit-lines in response to the voltages A and B. Nodes A and B are amplified by the P1-N1-P3-N3 inner positive feedback arrangement during the write operation by reflecting the bit-line voltages to them. Through a positive feedback arrangement of P2-N2-P4-N4, the amplified nodes A and B are sent back to complete the development of nodes C and D.

A single nFET and a single pFET, with their gates pinned to distinct nodes, provide the driving current for each of the four nodes in Quatro-10 T, just as they do in DICE. This allows for robustness in the face of disruption at a single node. If the data is "1," then node B should be VDD, node A should be 0 V, node C should be VDD, and node D should be 0 V. As a result of the shock, B may be inadvertently lowered below 0 V, which would cause N1 and N4 to shut down. However, turning off these transistors has no effect on the voltage at any of the other nodes. Instead, P3 provides the current to the reduced B by keeping D at 0 V. Since B is now at its original high value, the data "1" state has been restored.

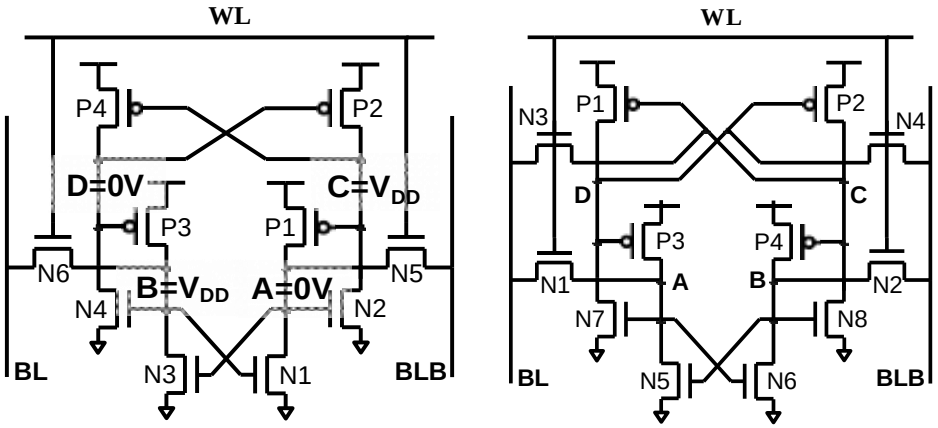

Figure 3. Schematic of (**a**) Quatro-10 T and (**b**) WE-Quatro-12 T SRAM cell.

Quatro-10 T, on the other hand, has a tolerance range of just 1.0 SEU to 0.0 SEU. As an example, when the value "1" is stored, B should be held at 0 V. Under these circumstances, B is susceptible to a SEU in the range of 0 V to VDD. As a result, nodes A and D are pulled down and N1 and N4 are activated. D's reduced potential may raise C through P2, which then cuts power to P1. With both P1 and N1 off, the node A may be brought down more quickly. As a result, the data flip happens, and the cell cannot restore itself to its original state.

Quatro-10 T also has a very limited capacity to write at low voltages. Nodes A and B, which originally store 0 V and VDD, should see a correct reflection of the data when the value "0" is changed to "1" in the hold cell (BL = VDD and BLB = 0 V). However, because of the Vth decrease, the node A is only weakly pushed up via N5; this has a knock-on effect of turning on N2 only weakly and pulling down the node C insufficiently to raise the node D. Therefore, P3 stays on and blocks N6 from bringing the B node down far enough. Therefore, the Quatro-10 T cell has very little room for writing.

A write-enhanced Quatro-12 T cell (WE-Quantro-12 T) is suggested [13], as seen in Figure 3b, to address the issue of limited write capabilities in the Quatro-10 T cell. Nodes C and D may now link to bit-line pairs through two more access transistors, N7 and N8. As a result, node D may be readily brought up to disable P3 in the previously specified data "0" write condition. The capacity to put pen to paper is much improved in this way. Weaknesses include a lack of error tolerance for the 0 to 1 flip of nodes A and B, much as in Quatro-10 T.

3.2.1 Radiation-Hardened SRAM Cell (RHD-12 T), Radiation-Resistant SRAM Cell (RHR-10 T), and PMOS-Stacked 10 T SRAM Cell (PS-10 T).

Figure 4a,b depict the radiation-hardened functioning of a PMOS-stacked 10 T SRAM cell and an NMOS-stacked 10 T SRAM cell, respectively [14]. PS-10 T's architecture is very similar to that of Quatro-10 T, with the exception that in PS-10 T, the nodes D and C are linked to the MP3 and MP1 sources rather than VDD. This resemblance also extends to the read/write processes, which are almost identical to those in Quatro-10 T.

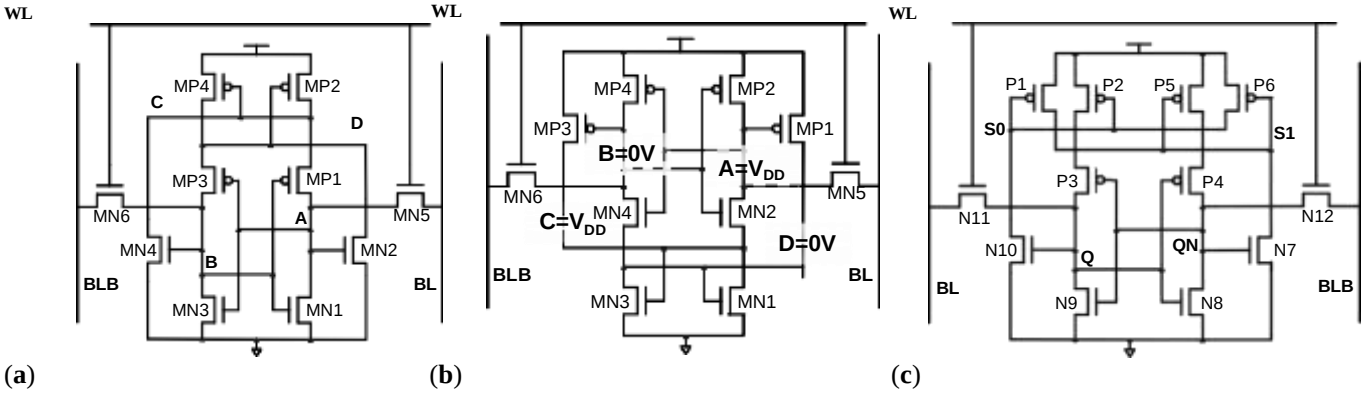

Figure 4. Schematic of (**a**) PS-10 T, (**b**) NS-10 T, and (**c**) RHD-12 T SRAM cell.

PS-10 T and NS-10 T, like Quatro-10 T, have limited SEU robustness. Recovery of 0-1 SEU is impossible in PS-10 T, whereas recovery of 1-0 SEU is impossible in NS-10 T. For instance, SEU may inadvertently reduce node A's voltage if NS-10 T records datum "1," indicating that the nodes' voltages are comparable to A = VDD, B = 0 V, C = VDD, and D = 0 V. As a consequence, MP1 and MP4 are activated, and nodes B and D increase in height. This allows MN1 and MN2 to statically drive A to 0 V, flipping the data, through the pull-down route of A.

The radiation-hardened design of a 12 T SRAM cell (RHD-12 T), described in [3], is seen in Figure 4c. This design is analogous to the PS-10 T structure. The sources P3 and P4 in RHD-12 T are not powered by S1 and S0 as they are in PS-10 T. In its place, S0 and S1-gated new components P2 and P5 are introduced to control P3 and P4. Both the P2-P3 and P5-P4 stacks can accommodate the shallow trench isolation. By doing so, we may prevent a node flip from occurring at P3 and P4 since charges gathered at drain nodes P2 and P5 cannot be injected into source nodes P3 and P5 through SEU. While PS-10 T cannot be retrieved from a SEU induced to "0" that stores the Q or QN nodes, RHD-12 T suffers the same fate.

The Radiation-Hardened-by-Design SRAM Cell (RHBD) is available in 10 T and 14 T versions.

The only acceptable ratios in Quatro-10 T, PS-10 T, and NS-10 T are 1 to 0 and 0 to 1. In contrast, the 1 to 0 and 0 to 1 SEU robustness of the radiation-hardened-by-design 10 T SRAM cell (RHBD-10 T) [15] is shown in Figure 5a. In comparison to Quatro-10 T, pFETs P5 and P6 are used in lieu of nFETs N2 and N4 in Figure 2 to drive the C and D nodes. Because of this modification, RHBD-10 T may now tolerate either a 1 or 0 SEU.

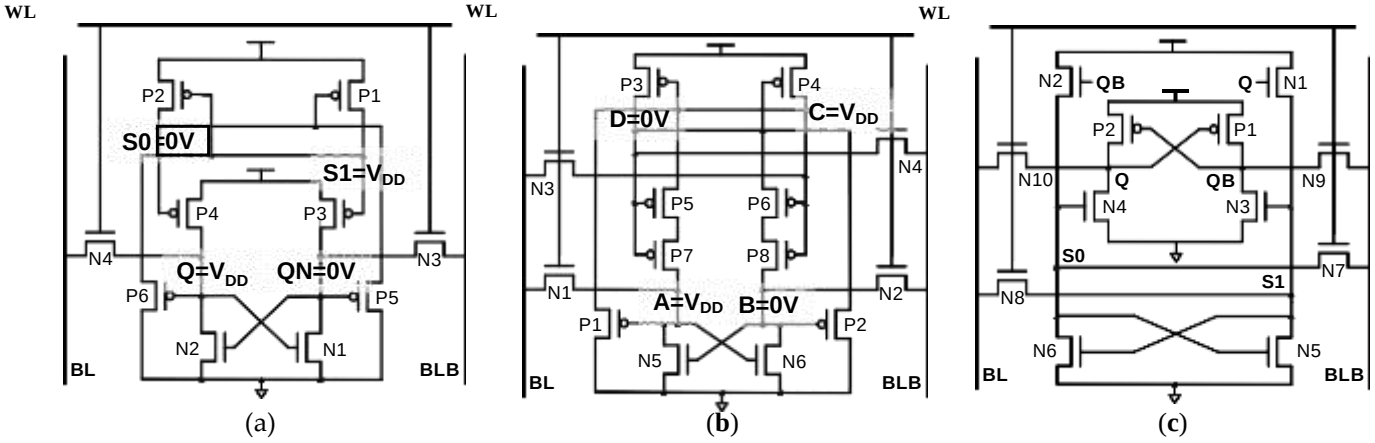

Figure 5. Schematic of (**a**) RHBD-10 T, (**b**) RHBD-14 T, and (**c**) RHPD-12 T SRAM cell.

For RHBD-10 T, for instance, Q = S1 = VDD when the value "1" is saved, whereas QN = S0 = 0 V is recorded when "0" is stored. The QN of RHBD-10 T may experience an upset of magnitude 0 to 1. By doing so, N2 is activated, briefly reducing Q. QN is raised to VDD, but when P4 is left on, it pushes Q back down to 0 V. This indicates that a Q or QN may recover from a 0-1 upset.

The Q or QN node might also experience the 10 upset. When the value "1" is saved, for instance, Q may be reduced from VDD to VDD-1 because of the 1-to-0 SEU. Then, P6 is accidentally activated, causing S1 to drop. P1, which is greater in size than P6, is activated to maintain S1's high state, while P6, being a pFET, can only weakly transmit a "0" to S1. As a result, P2 won't activate and S1 will continue to rise. Therefore, S0's voltage remains at 0 V to maintain P4's on state. Finally, activating P4 restores 1 to 0 SEU by inverting Q back to its starting voltage of VDD.

Since only pFET diffusions are linked to the S0 and S1 nodes and not nFET diffusions (drains or sources), 1 to 0 SEU is impossible at these nodes. Therefore, a transition from 0 to 1 has no effect on the S0 or S1 nodes since it does not activate any transistors. If S0 or S1 is accidentally increased by SEU, the value is reset to 0 when P6 or P5 is activated.

Despite being resistant to many kinds of single-node disturbance, RHBD-10 T's limited write ability is its fatal flaw. N4 transfers BL = 0 V, hence in the case when datum "0" is to be written for the datum "1" stored cell, Q should be decreased to 0 V. To ensure that Q is reduced, S0 must be raised, at which point P4 must be turned off, and P2 must be switched on. In order to activate P2, however, S1 must be reduced, which is a formidable challenge for RHBD-10 T. This is because pFET P6 ought to be responsible for pulling S1 down, not nFET. As a result, RHBD-10 T has a much higher chance of failing while writing in low-voltage or high-frequency settings.

Figure 5b depicts RHBD-14 T, which is offered in [16] as a solution to the write failure issue with RHBD-10 T. The addition of N3 and N4 to improve writing speed is the most noticeable alteration. This method is analogous to the manner in which WE-Quatro-12 T fixes the issue of Quatro-10 T's limited writing capacity. Since N3 pulls down node C directly, turning off P5 and P7 at the same time is easier when D is elevated. To further improve error robustness through the charge-sharing effect, RHBD-14 T uses a stacked design of pFETs to drive either the node A (P5-P7) or node B (P6-P8).

Nodes C and D of RHBD-14 T are not SEU-tolerant, in contrast to RHBD-10 T's 100% tolerance for SEU. Data "1" stores the values A = C = VDD, B = D = 0 V, and allows node C to be lowered by SEU, which in turn raises node D via the activated P3. N4 lowers the node A since P6 and P8 are now on, which also raises the node B. As a result, we activate P1, which makes node C low. As a consequence, the formerly "1" information will now be "0."

The issue of RHBD-10 T's poor write ability may be addressed in another way. In Figure 5c, we can see the internal workings of the radiation-hardened polar design (RHPD-12 T) of the SRAM cell [17]. Adding two more transistors, N7 and N8, allows for direct access to the internal storage nodes, making RHPD-12 T the polarity-inverted counterpart of RHBD-10 T. Complete tolerance to SEU may be preserved in this way while the issue of write failure is greatly alleviated.

However, the driving strengths of N3 and N4 are decreased during the read operation when either S0 or S1 stores a weak "1." As a consequence, the low-voltage area experiences a drastic narrowing of the read stability margin, leading to an unfeasibly high risk of data flipping during the read operation.

3.2 RHBD-12 T Radiation Hardened SRAM Cell

The radiation-hardened-by-design 12 T SRAM cell (RHBD-12 T) is shown in a simplified form in Figure 6 of [18]. No nFET diffusion nodes are coupled to Q and QB through pFET access transistors; this is the defining structural characteristic of RHBD-12 T. The range, then, is from 1 to

The Q and QB nodes do not cause any disturbance, and the little amount of upset that does arise may be easily fixed. As illustrated in Figure 6, QB may be momentarily elevated by SEU, which activates N4, when Q = S1 = VDD stores the data "1" and QB = S0 = 0 V. P8 is now in a disabled state, therefore there is no impact on any other storage nodes. When the QB is elevated, the P7-N2 route acts to bring it back down to ground level.

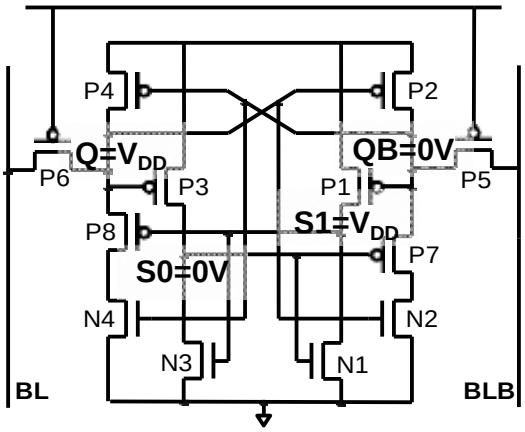

Figure 6. Schematic of RHBD-12 T SRAM cell.

The S0 or S1 node, in contrast to the Q or QB node, is susceptible to both 0-1 and 1-0 node upsets. But the following is how to get back on track after such disruptions. As a first step, P8 is activated and N3 is deactivated if the 1 to 0 upset happens at node S1 for the data "1" state. Even when P8 is activated, Q is not lowered since N4 is not now engaged. As a result, S1 is brought back up to VDD while P1 remains on and QB is maintained at a low level. Second, if an upset from 0 to 1 happens at node S0 for the "1" data state, N1 is momentarily activated to briefly draw down node S1, activating P8. However, N4 is still off, high Q is unaffected, and QB may be kept at a low setting. As a result, S1 is brought back up to VDD, while S0 is brought back down to 0 V. Because of its reliance on the pFET access transistor and the pull-down transistor, RHBD-12 T suffers from a lengthy read access time. The cell current flows via P5-P7-N2 and discharges the BLB, allowing for the "1" to be read. When BLB is discharged, the amplitude of VGS in access transistor P5 and pull-down transistor P7 decreases, which significantly slows down the read operation compared to other memory cell architectures. Furthermore, the write speed and stability are both drastically reduced when pFET transistors are used.

3.2 QUCCE-10T and QUCCE-12T, Quadruple Cross-Coupled Latch-Based 10T and 12T SRAM Cell

Figure 7a,b depicts the architecture of a 10 T (QUCCE-10 T) and 12 T (QUCCE-12 T) SRAM cell, respectively [19]. Data is stored in the four nodes A, B, Q, and QN, as in earlier SRAM cell layouts, and the pFET and nFET transistors whose gates are coupled to the various nodes power the circuit. In this case, a complete positive feedback network for data storage is formed by the four cross-coupled FETs.

However, compared to other radiation-hardened SRAM cell designs, the SEU tolerance of QUCCE-10 T is much lower due to its complete positive feedback. If the voltage at any storage node is altered by a SEU, the positive feedback will be activated, amplifying the original voltage shift. For the "1" data stored cell with A = 0 V, B = VDD, Q = VDD, and QN = 0 V, a 0 to 1 SEU on the QN node is possible, causing the Q node to be pulled down. This activates P1, which pulls up node A, which in turn activates N4, which in turn pulls down node B. P3 is activated, which further increases QN's voltage increase.

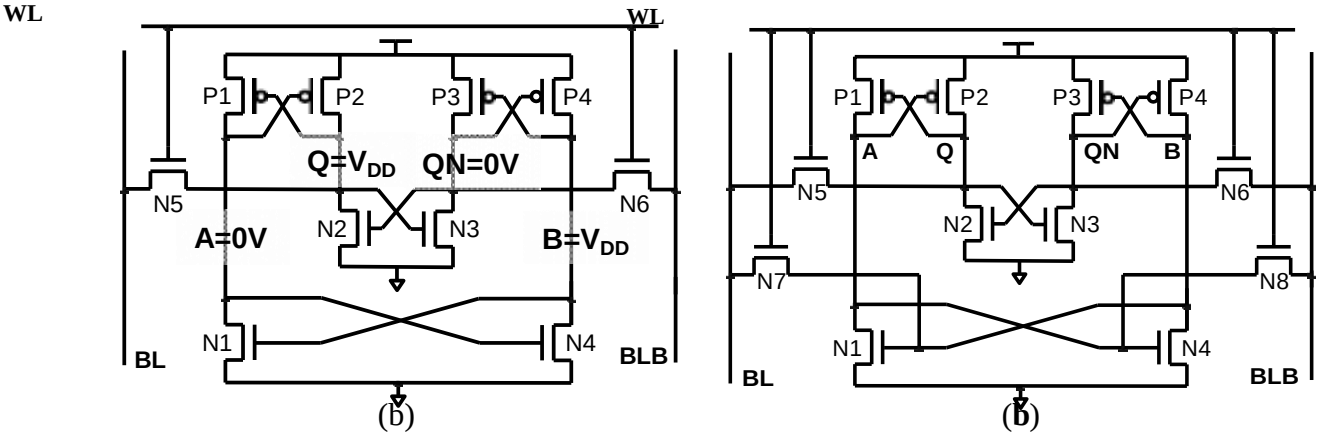

Figure 7. Schematic of (**a**) QUCCE-10 T and (**b**) QUCCE-12 T SRAM cell.

Design Approaches to Reduce Area/Power

The most popular design is the DICE- 12 T, however several designs have been created to reduce its space and power needs. Many structures with fewer transistors (including Quadro-10 T, NS-10 T, PS-10 T, RHBD-10 T, and QUCCE-10 T) make use of the four store nodes; however, only two storage nodes are accessible by two access transistors. Two individually controlled FETs power each of the four storage nodes to VDD and 0 V, providing radiation hardening. The data is stored in a positive-feedback architecture with the four storage nodes consisting of two or more cross-coupled nFETs or pFETs. These designs reduce the overall number of transistors, and hence the amount of room and power they need. However, in these designs, the internal storage nodes that are vulnerable to dropping and increasing SEU are being driven directly by cross-coupled nFETs or pFETs that are storing the data. Therefore, even little charge noise is enough to trigger the positive feedback, which might cause a reversal of data. Due to their low QC values, these structures are vulnerable to SEU. This is especially true of the NS-10 T, PS-10 T, and RHBD-10 T.

These designs also suffer from slower write speeds and higher write latency. When an access transistor tries to change the voltage of a storage node, a high contention current flows through it. This is because of how the radiation hardening setup is set up; specifically, how individual signals are sent to the FETs that power a single storage node. The cell designs also have little resistance to SEU since four storage nodes are housed inside the positive feedback structure.

Techniques for Designing Durability, Comfort, and Increased Writing Capacity 3.3

All four storage nodes may be accessed through bit-lines in certain designs, such the WE-Quatro-12 T, RHPD-12 T, RHBD-12 T, and QUCCE-12 T, which boosts write performance. A bigger physical size and more energy consumption are inevitable consequences of the additional two transistors and supporting circuitry.

One common technique for increasing SEU tolerance is to have the storage node of the bitcell constructed with just increasing or decreasing SET. Since a falling SET won't turn on any transistors, the SEU may be prevented if the node that detects it is connected to a nFET. Both the RHPD-12 T and the RHBD-12 T may employ four access transistors to increase their SEU resistance, and only nFET or pFET diffusions are required at the storage nodes. When just one kind of FET (pFET or nFET) is utilized at a node, the drivability will always be compromised (because the device can only be driven in one of two states, 1 or 0). As a result, certain structures' functionality and steadiness suffer severely.

3.4 Using a Changing Node as a Refresh Signal

Increased SEU tolerance may be achieved, for instance, in RHPD-11 T and RHD-11 T by combining the refresh process with the use of an isolated dynamic storage node. Combining these architectures with a Schmitt trigger inverter to produce RHPD-13 T and RHD-13 T may also increase tolerance for multiple node upsets. However, single-ended bit-line is used to cut down on bulk, which slows down read/write operations. The production of control signals for the refresh process takes much more work.

In particular, the devices' limited capacity for writing is due to their single-ended design. Since M9 only enhances "1" write stability, it is used as a workaround by RHBD-11 T and 13 T. Both RBD-11 T and 13 T have limited writing capabilities due to the usage of nFET pass-transistors in lieu of transmission gates for access. Although it would take up more room, this problem may be solved by using a pFET header switch for M9 or the transmission gate.

In the future, SRAM cells will need to prioritize high read/write performance and robust SEU tolerance. This is because there have been several problems with the reliability of the SEU vs the read/write performance of the memory in the SRAM cell designs that have been offered in the past. Moreover, as technology decreases in size, the need of finding solutions to the various node upset concerns will grow. The use of a dynamic node with refresh signals would be severely hampered in sub 10-nm technology nodes due to increased degrees of uncertainty and smaller device dimensions. So, it's important to create designs for static SRAM cells that can endure recurrent node upset.

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